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Applicant : Albrecht Mayer

Applic. No. : 09/164,123

Filed : September 30, 1998

Title : Method for Assembling Integrated Circuits
With Protection Of The Circuits Against
Electrostatic Discharge, And Arrangement Of
Integrated Circuits With Protection Against
Electrostatic Discharge

Examiner : Kurt M. Eaton

Group Art Unit : 2823

TECHNOLOGY
FEB-5

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Hon. Commissioner of Patents and Trademarks,
Washington, D. C. 20231

S i r :

Responsive to the Office action dated June 4, 2001 kindly
reconsider the above-identified application as follows:

Reconsideration of the application is requested.

01/31/2022
01 Feb 16

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Claims 1-11 and 16-18 remain in the application.